

ABSTRACT OF THE DISCLOSURE

Clock processing logic and method for determining clock signal characteristics in reference voltage and temperature varying environments are described. A sample vector is characterized by bit locations corresponding to sequentially increasing delay values so that values stored in such bit locations indicate clock signal edges where value transitions occur. In one embodiment, edge detection logic and sensitivity adjustment logic are used in determining the clock period from such a sample vector. In another embodiment, an edge filter, sample accumulation logic, and clock period and jitter processing logic are used in determining an average clock period and clock jitter from a predefined number of such sample vectors.